Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.085”**

**.051”**

**TR14**

**126A**

**12 11 10 9**

**8**

**7**

**6**

**3 4 5**

**13**

**14**

**1**

**2**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: FLOATING**

**Mask Ref: TR14 126A**

**APPROVED BY: DK DIE SIZE .051” X .085” DATE: 5/16/19**

**MFG: HARRIS THICKNESS .015” P/N: 54ACT32**

**DG 10.1.2**

#### Rev B, 7/1